1. (Twice Amended) A liquid crystal display (LCD), comprising:

a gate line formed on a transparent substrate, edges of said gate line being substantially straight and even;

a data line crossing said gate line and formed on said transparent substrate, edges of said data line being substantially straight and even;

an insulating layer electrically insulating said data line from said gate line;

a thin film transistor formed at an intersection of said gate line and said data line, and connected to said gate line and said data line;

a passivation layer formed over the thin film transistor;

a pixel electrode formed on the surface of the passivation layer; and

a low reflective layer formed on at least a portion of at least one of said gate line and said data line.

15. (Twice Amended) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and a portion protruding from said gate line to serve as a gate electrode of a thin film transistor on a transparent substrate, edges of said gate line being substantially straight and even;

forming an insulating layer electrically insulating said gate line;

forming a data line over said transparent substrate and crossing said gate line, edges of said data line being substantially straight and even;

forming a passivation layer over the thin film transistor;

forming a pixel electrode on the surface of the passivation layer; and

first forming a low reflective layer over at least a portion of at least one of said gate line and said data line.

22. (Twice Amended) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and gate electrode connected thereto on a transparent substrate, edges of said gate line being substantially straight and even;

forming an insulating layer over said gate line and gate electrode;

forming a semiconductor layer over said gate electrode;

forming a data line crossing said gate line, edges of said data line being substantially straight and even, a source electrode connected to said data line and on a first portion of said semiconductor layer, and a drain electrode on second portion of said semiconductor layer;

forming a low reflective layer over at least a portion of at least one of said gate line and said data line;

forming a passivation layer having a contact hole exposing said drain electrode over said transparent substrate; and

forming a pixel electrode on said passivation layer and connected to said drain electrode via said contact hole.